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(Marcus J. Millet)

Docket No.: TESSERA 3.0-085 CONT DIV CIP (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re Patent Application of:
Joseph Fjelstad

Application No.: 09/732,821

Filed: December 8, 2000

For: METHODS FOR MANUFACTURING
RESISTORS USING A SACRIFICIAL
LAYER

Commissioner for Patents
Washington, DC 20231

Group Art Unit: 2814

Examiner: A. Chappell

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AMENDMENT

Dear Sir:

In response to the official action mailed December 14, 2001, applicant submits the following amendments and remarks.

IN THE ABSTRACT:

Delete the Abstract of the Disclosure in its entirety as it appears on page 45 and substitute therefor the Abstract set forth on the attached page.

IN THE SPECIFICATION

CLEAN COPY OF AMENDED SPECIFICATION PARAGRAPHS:

Paragraph [0016] is amended to read as follows:

[0016] FIG. 1E-2 shows a top view of FIG. 1D-1 in which several chips are back-bonded to a sacrificial layer and electrically connected thereto prior to the encapsulation step, according to the '671 disclosure.

Paragraph [0044] is amended to read as follows:

[0044] In FIG. 1B, a plurality of pads 110 are selectively formed, typically by an electroplating operation, so that the

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Level

pads 110 are disposed on and attached to the first surface 101 of the sacrificial layer 100. The pads 110 are arranged on the first surface 101 of the sacrificial layer 100 so as to define a central region 114 between the pads of a particular package group. The pads may be arranged in single rows around the central region 114 or may be arranged in multiple rows in a substantially grid array arrangement, an example of which is shown in FIG. 1D-2. The pads 100 in this embodiment are comprised of a first layer of copper 111 and a second layer of gold 112. Typically, there is also a center barrier layer (not shown) of nickel to ensure that the copper and gold layers do not diffuse into one another. The gold layer 112 facilitates a bond that is made by the electrical connection to the chip contacts, as described in more detail below. The height of the pads 110 is not critical so long as a good electrical connection can be made thereto. In some embodiments, the pads may resemble posts. Other examples of permissible pad materials include copper, nickel, gold, rhodium, platinum, silver and alloys and combinations thereof. Typically, in a low pin count package, the pads 110 are all of the same height from the sacrificial layer 100. However, for higher pin count packages or for other reasons, the pads 110 may not all be of the same height from the sacrificial layer 100. Taller pads 110 can be used in outside rows of pads to ensure that the electrical connections between the contacts and the inner pads do not electrically short with the connections between the contacts and the outer pads. This can be useful in cases where the chip contacts are finely spaced or where the contacts are arranged in an area array on the face surface 121 of the chip 100, an example of which is shown in FIG. 1D-2.

Paragraph [0046] is amended to read as follows:

B3 [0046] Next, the chip contacts (not shown) on the face surface 121 of the chip 120 are each electrically connected to a respective pad 110 by wirebonding the one to the other, as shown in FIG. 1D-1. The wirebonded connection 130 could take the form of a ball bond/stitch (or wedge) bond combination, as shown, or the wire could be stitch-bonded to both the chip contacts and the pads 110. Other conventions could be used to interconnect the chip contacts and the pads, such as TAB leads, electroformed beam leads, etc. FIG. 1E-2 shows a top view of FIG. 1D-1.

[Paragraph [0047] is amended to read as follows:]

[0047] The assembly, including the first surface 101 of the sacrificial layer 100, the pads 110, the chip 120 and the electrical connections, is next encapsulated (or over-molded) by a flowable, curable dielectric material 140, as by convention semiconductor molding technology, as shown in FIG. 1E. The dielectric material is typically comprised of filled or unfilled standard thermoset or thermo plastic resins as used in the industry, such as epoxy resin, silicone resin or other plastic encapsulating material. The dielectric material is then fully cured.

Paragraph [0049] is amended to read as follows:

A4 [0049] In FIG. 1G-1, the individual packaged chips 150 are "diced" or separated from each other. At this point, the exposed bottom surfaces 113 of the pads 110 may be attached to respective bond pads on the PWB. One method of making such an attachment is to connect solder balls to the bottom surface 113 of the pads 110. The solder balls are typically comprised of a combination of tin and lead and may further coat a solid metal ball such that the solder balls are non-collapsing. FIG. 1G-2 shows a bottom view of a multichip module embodiment of the '671 disclosure in which the packages are diced so that more than one

chip 120 is included in the resulting package. FIG. 1G-2 could also be the top view of the undiced packages, as shown in FIG. 1F. While the above process is shown and described in an embodiment that packages more than one chip simultaneously, the process could also be used to package an individual chip if desired.

[Paragraph [0050] is amended to read as follows:]

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[0050] In an alternative method of manufacture shown in FIGS. 2A-E, the sacrificial layer is comprised of a dielectric polymer sheet 100' having a conductive layer 101', typically a thin layer of copper, on one surface of the sacrificial layer 100', as shown in FIG. 2A. An array of conductive pads 110' are next photo-lithographically defined by etching away undesired sections of the conductive layer 101' so that the pads 110' define a central region 114' therebetween. Within the central region 114', a central conductive region 115' may also be defined by the pad-forming lithographic process, as shown in FIG. 2B. A back surface 122' of a semiconductor chip 120' is then bonded to the conductive region 115' through the use of the thermally conductive die attach adhesive 135', as discussed in reference to FIG. 1. The chip contacts (not shown) on the exposed face surface 121' of the chip 120' are then electrically connected to respective pads 110' by wirebonding wires 130' therebetween. As discussed above, the elements are next encapsulated in FIG. 2D using a suitable liquid encapsulant for the application and the encapsulant 140' is cured. Portions of the polymer sheet 100' are then removed, as by chemically etching or laser ablation operations, so that the pads 110' and central conductive region 115' are exposed. The packages may then be diced into either individual packages or multichip packages and connected to a PWB with conventional solder. Typically, the central region 115' is connected to the PWB in

such a way that heat is drawn away from the chip into the PWB during operation of the package. As shown in the top plan view of FIG. 2F, a multichip package may include chips of different sizes that perform different functions. The addition of a dielectric, polymer sheet 100' allows this multichip module to have conductive paths 118' interconnecting at least some of the pads 110' within the multichip module thereby allowing signals to be transferred between the chips. It should be noted that if a wiring layer, such as is described in this multichip embodiment, is not needed or desired, the entire polymer sheet 100' may simply be removed by chemically dissolving the sheet leaving the pads and the central conductive region exposed.

Paragraph [0051] is amended to read as follows:

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[0051] FIG. 3 shows a still further embodiment of a packaged chip, similar to the packaged chips shown in FIG. 1G-1. In FIG. 3, however, a conductive protrusion 116' is electrically connected to a respective pad 110' and extends to the top surface 155' of the finished package 150' so that a top surface 117' of the protrusion 116' is exposed. This arrangement allows the bottom surface 113' of the pads 110' to be soldered to a supporting substrate (such as a PWB) while allowing another electronic component and/or semiconductor chip to be electrically connected to the packaged chip via the exposed top surface 117' of the protrusions 116'; thus, creating a chip stacking technique. The protrusions may extend from every pad; however, typically they will extend from less than all of the pads.

Paragraph [0052] is amended to read as follows:

[0052] In a further embodiment, FIG. 4A shows a side view of a microelectronic component 170'' which is attached to the chip 120''. The contacts on such a microelectronic component may be electrically connected between respective contacts on the chip

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120'' and/or may be connected to respective pads 110''. Where the microelectronic component is a second semiconductor chip 170'', as shown in FIG. 4B, the back surface of the second chip 170'' will be back-bonded to the face surface of the first chip 120'' and the contacts on the second chip may be electrically connected to the contacts on the first chip 120'' and/or to respective pads 110''. The pads 110'' themselves may also be electrically interconnected.

Paragraph [0054] is amended to read as follows:

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[0054] Conductive pads 210 are next plated into the cavities 203 and apertures 205 so as to create the rivet-like pads 210, as shown in FIG. 5C. These pads 210 have a bottom bump flange 213 adjacent to the sacrificial layer 200 and integrally attached to a post pad 211 such that the post pad protrudes from the bump flange 213. A second bump flange 212 is integrally attached to the opposite end of the post pad 211. Both bump flanges 212/213 have flange areas that extend beyond the diameter of the post pad 211. FIGS. 5I-5J show alternate cross-sectional pad configurations, according to the present invention. In the embodiment shown in FIG. 5I, the pad is comprised of the bottom bump flange 213' and the post pad 211', depicted in conjunction with sacrificial layer 200'. In FIG. 5J, the bump flanges 212'' and 213'', shown in conjunction with post pad 211'' and sacrificial layer 200'', are more squared off at the edges when compared to the rounded/oval bump flanges shown in the other FIGS. Other shape bump flanges may also be used.

[Paragraph [0055] is amended to read as follows:]

[0055] In FIG. 5D, the photo-imageable layer 204 is removed leaving the pads 210 such that the pads within a particular group define a central region therebetween. A chip 220 is next

back-bonded to the first surface of the sacrificial layer 200 using a thermally conductive die attach adhesive 235, as described in the previous embodiment. FIG. 5E shows electrical connections 230 interconnecting the chip contacts (not shown) on the face surface 221 of the chip 220 and the pads 210. The electrical connections 230 are made by using a wirebonder to stitch bond both ends of the wire to the pad 210 and the chip contacts. The stitch bonds create a low profile electrical connection between the contacts and the pads that, in turn, allows the finished package to be thinner. The pads 210, chip 220, and wires 230 are then encapsulated using an encapsulant 240, as described above in reference to FIG. 1 and further shown in FIG. 5F. The sacrificial layer is next etched away to expose the bottom bump flange 213, as shown in FIG. 2G. The packaged chips are then diced into either individual packaged chips or packaged multichip modules, as shown in FIG. 5H.

[Paragraph [0056] is amended to read as follows:]

[0056] In a still further embodiment, FIGS. 6A-6F show another stackable chip arrangement. FIG. 6A-1 shows a side view in which a dielectric base material layer 305 is disposed on a top surface 302 of a sacrificial layer 300. The base material 305 is preferably comprised of a dielectric sheet-like layer, such as polyimide. Typically, the base material 305 is laminated onto the sacrificial layer 300. Conductive pads 310 are disposed on the base material 305. The pads 310 may be plated on the base material 305 prior or subsequent to the base material's attachment to the sacrificial layer 300. FIG. 6A-2 shows a top plan view of FIG. 6A-1. The pads 310 in FIG. 6A-2 have bonding sites 315 and via sites 316. The pads 310 further define a central cavity 314. As shown in FIG. 6B-1, a semiconductor chip 320 is then back-bonded to the first surface 302 of the sacrificial layer 300 within the central cavity. The

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chip contacts (not shown) are next electrically connected to respective bonding sites 315 on the pads 310. Typically, the contacts are connected to the respective bonding sites 315 by wire bonds 330. FIG. 6B-2 shows a top plan view of FIG. 6B-1.

[Paragraph [0080] is amended to read as follows:]

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[0080] After formation of the shells 906 the apertured layer 903 is removed from the first surface of the sacrificial layer 900, as shown in FIG. 9E. Next, as shown in FIG. 9F, a layer 907 of resistive material is deposited, using any of the methods previously described, over the first surface 901 of the sacrificial layer 900 such that the resistive layer 907 covers the first surface 901 of the sacrificial layer 900 and fills the interior spaces 911 of the shells. Thus, each shell or pad 906 and the resistive material 908 (Fig. 9G) within the shell forms a projection extending from the bottom surface of the resistive layer.

[Paragraph [0093] is amended to read as follows:]

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[0093] In an alternative embodiment, as shown in FIG. 12, a non-conductive apertured layer 1210, which is thicker than the patternable layer used in the embodiments shown in FIGS. 8A-8I, is applied across the first surface of the sacrificial layer. Pads 1230 and posts 1240 are formed as discussed above with reference to FIGS. 8A-8I, so that the top bump flanges 1231 are initially in contact with the surface of the apertured layer. The apertured layer 1210 is etched or dissolved from the first surface of a sacrificial layer (not shown). However, the etching or dissolving process is arrested before the entire apertured layer 1210 has been removed. and a portion of layer 1210 remains on the first surface of the sacrificial layer. For example, if the apertured layer 1210 is comprised of a polyimide, a hot caustic solution can be used to remove a portion of the patternable layer 1210. An etch rate may be selected for the

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hot caustic solution such that only a portion of the patternable layer is removed.

Paragraph [0097] is amended to read as follows:)

GA [0097] As shown in FIG. 14, a resistive device 1400 according to a further embodiment of the invention includes pads 1402, resistive layer 1403 and a heat sink 1404 overlying the top surface of the resistive layer, remote from the pads 1402. The heat sink 1404 is formed from a thermally-conductive material such as, for example, aluminum. Where the material of the heat sink is electrically conductive, a thin dielectric layer 1408 is provided between the base surface 1406 of the heat sink 1404 and the resistive layer 1403. For example, the base surface 1406 of the heat sink may be treated with an insulating finish such as epoxy or anodized. Alternatively, a dielectric layer may be provided on the resistive layer as, for example, by a molding process as discussed above with reference to Figs. 11A-11E, or by laminating the dielectric layer to the resistive layer. In a further variant, the heat sink and dielectric may be provided as a unit which is applied in place of a simple dielectric layer in a molding process as described with reference to Figs. 11A-11E. The heat sink 1404 allows the resistive device 1400 to dissipate more power without overheating. While the resistive device 1400 as shown in FIG. 14 is manufactured by the method as shown in FIGS. 9A-9H, resistive devices manufactured by any other method of manufacturing resistors described herein may be mounted onto a heat sink in similar fashion.

Insert new paragraph [0016.1] in the specification to read as follows:

GA [0016.1] FIG. 1D-2 is a top plan view of a chip and sacrificial layer according to another embodiment.

IN THE CLAIMS